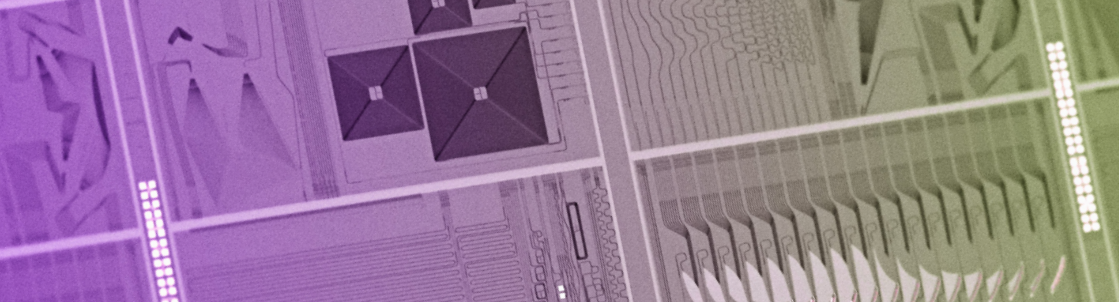
VTT

beyond the obvious

Silicon photonics MPW offering 2020



VTT offers its 3 µm silicon photonics platform in biannual, open access multi-project wafer runs. The runs are optimal for low-cost, low-barrier prototyping of photonic integrated circuits and for evaluating the use of 3 µm silicon-on-insulator technology for specific applications.

Chip sizes and pricing model

Two design area sizes of 5×10 mm² and 20×20 mm² are offered in the MPW runs. The base price includes the delivery of either 8 identical chips from the 5×10 mm² design, or one chip from the 20×20 mm² design. With the same design, each additional delivery of either 8 identical chips of 5×10 mm² design, or one chip from the 20×20 mm² design, costs 50% of the basic price.

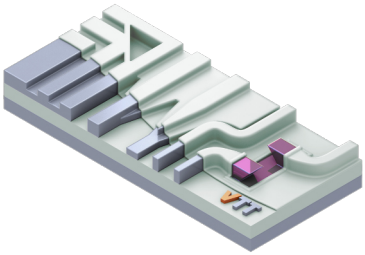
Design Support

VTT offers a process design kit (PDK) to end users participating in MPW runs to facilitate design work. This documentation consists of three PDF handbooks describing the process flow, design guidelines, and the design rules. Also provided is a sample GDS file with example building blocks, and corresponding support files for KLayout. A design library for VTT's MPW technology, including a number of basic building blocks, is available for Synopsys' OptoDesigner mask layout software.

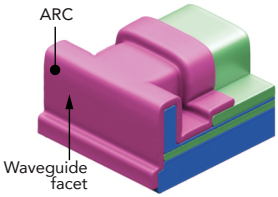
VTT also offers circuit design as an additional service, please contact us for pricing information.

How to Join

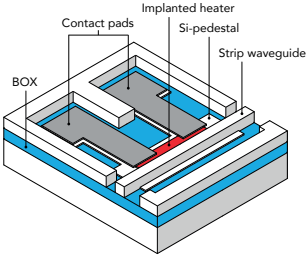
You can express your interest in joining an MPW run by sending an email to silicon.photonics@vtt.fi. Gaining access to the PDK documentation requires a signed design kit license agreement (DKLA) or a similar agreement with VTT. The DKLA can be downloaded online at www.vtt.fi/siliconphotonics.



Rib and strip waveguides, low-loss converters and up-reflecting mirrors



Wafer level anti-reflection coating



Implanted heaters for thermo-optic tuning

MPW run offering 2020

Run 20-1 — Design deadline June 30th 2020

Process modules	Est. delivery	Base price	Maturity
Passive	September 2020	9 500 €	High
Active	November 2020	14 500 €	High

Run 20-2 — Design deadline December 1st 2020

DATES CHANGED

Process modules	Est. delivery	Base price	Maturity
Passive	March 2021	9 500 €	High
Active	June 2021	14 500 €	High
Active with Ge PDs	September 2021	32 000 €	Medium

A discount of 2000 € is applied to each additional order within the same MPW run.

The Ge PD process may be offered as an experimental module in 20-1 run, please contact VTT to check the availability and express interest in joining.

Description of the process modules

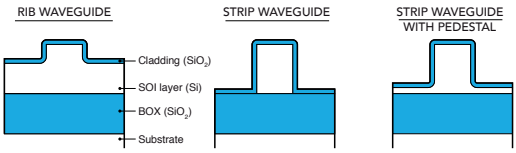
Passive module includes rib waveguides and two types of strip waveguides (through-etched and with ~200 nm thick pedestal for e.g. heaters in active module). Process also includes Al-coated facet reflectors to create resonators or to enhance echelle grating performance. Chip edges are deeply etched and AR-coated (1300 nm or 1550 nm) to support fiber array attachment and testing.

Up-reflecting TIR mirrors were introduced in the MPW process in 2019. The mirrors support wafer level testing with vertical I/O coupling to fibers and the integration of VCSELs and detectors.

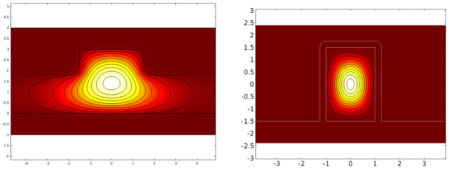
Active module has the same process steps as the passive module, but adds Al for electrical wiring and silicon implantation (p- and n-type) steps for heaters and PIN modulators.

Solder process for flip-chip integration of e.g. laser chips and detectors is available on request.

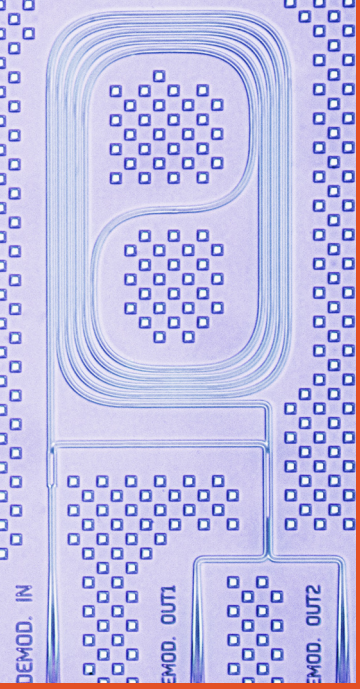
Ge photodiodes (Ge PDs) are introduced as a new functionality in the MPW process in 2020. Separate black box designs are available for monitor photodiodes (<1 GHz) and fast photodiodes (>1 GHz).

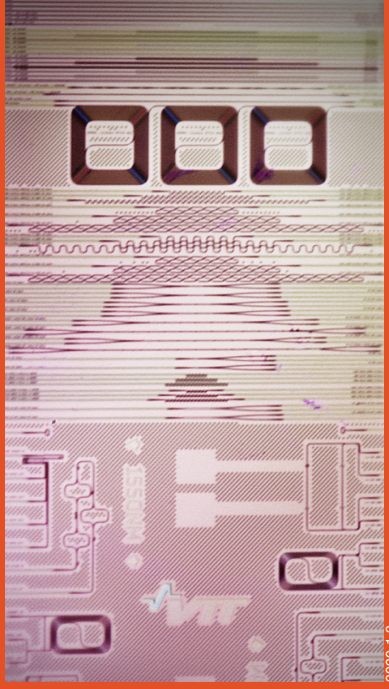


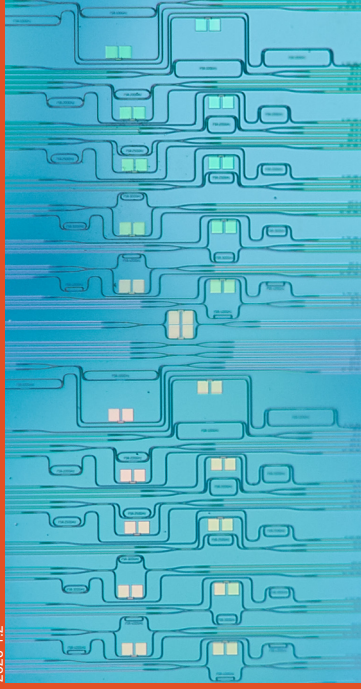
3 µm thick SOI waveguide cross-sections



Fundamental modes in a single-mode rib and multi-mode strip waveguide







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